CP 8xxx

with

Dual Ethernet Ports
for
Density Series Systems

User's Guide

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User's Guide
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Chapter 1 – Introduction

The Cubix Density Series System houses multiple server-class Intel® compatible computers neatly and efficiently in a single rack-mountable drawer (see Figure 1). The Density Series System is designed for the purpose of computer consolidation. Cubix equipment solves the problems associated with space-constrained backroom computing centers.

The CP8xxx is a Density Series processor board which can plug into any one of the independent groups on a Density Series backplane. "Group" refers to a segmented number of slots within the backplane that will accommodate a Density processor board and peripheral third party card(s), which comprise the server-class system. As many as eight CP8xxx Series boards can be installed in a Density System.

There are three steps to insure proper installation of the board. (1) Switch settings must be checked for proper configuration; (2) a power down of the group where the board will be installed must be done; (3) and the board must be inserted into the proper group slot.

This *User's Guide* provides details on switch and jumper settings, the steps necessary for proper installation of the board and information regarding the technical specifications of the CP8xxx board.

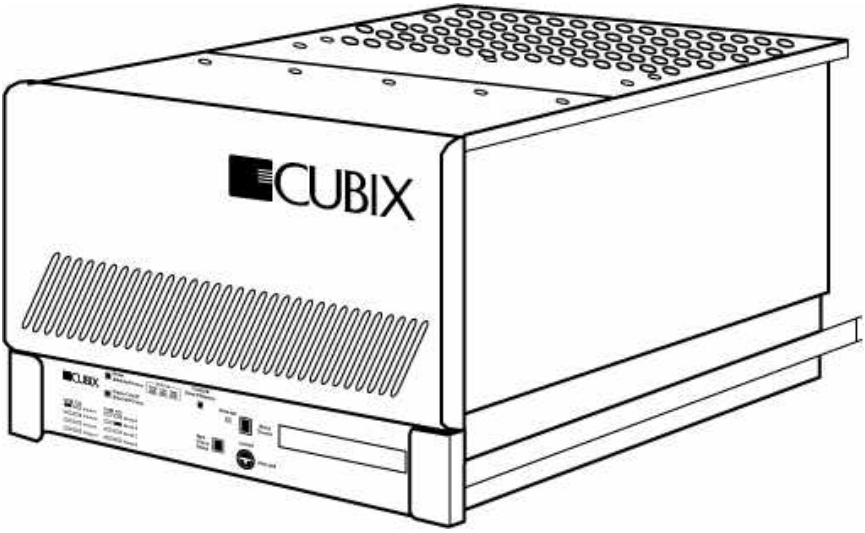

Figure 1 Density Series System

OVERVIEW

The CP8xxx board uses the Intel 440BX chipset and an Intel Celeron processor with speeds up to 500Mhz. There are two DIMM sockets for a maximum of 512MB of memory. This processor board uses a 66Mhz front side bus and a 33Mhz-PCI bus timing. The board is designed for the Density Series chassis which will hold up to eight of the CP8xxx boards. Figure 2 shows the board layout for the CP8xxx.

Once installed in a Cubix Density System, each CP Series board becomes an independent computer. The system multiplexor allows all Density computers in a chassis to share a single floppy disk drive and CD-ROM drive. The monitor, mouse and keyboard may be shared between groups and multiple chassis (up to 8).

CP Series computers include on-board video, two serial ports, one parallel port, keyboard and mouse support, memory and floppy drive support. Also included are two integrated Ethernet controllers with two 10/100 Base-TX connectors and an internal Ultra ATA/33 (EIDE) 48 pin mini-DIN connector. Optional is an integrated Wide Ultra2 SCSI controller with Single-Ended or Low Voltage Differential (LVD) support to an external SCSI connector. This board also supports PCI and ISA expansion slots.

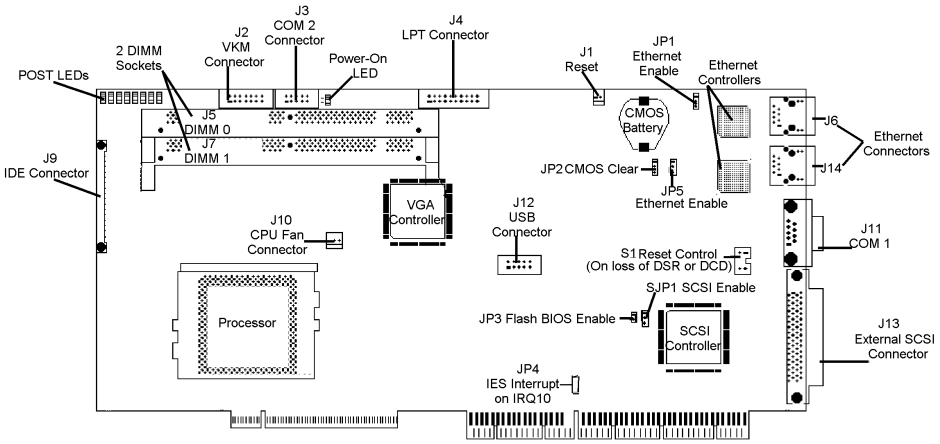

Figure 2 CP8xxx Series Board Layout

Chapter 2 – Switch and Jumper Settings, Memory Installation

S1 – Position 1

The CP8xxx board comes equipped with a 2 position dip switch for reset control. Position 1 is for data set ready (DSR). If position 1 is set in the "on" position (the "on" and "off" positions are designated by an arrow clearly marked on the switch), the CP8xxx board will reset the CPU on loss of data set ready. The factory default setting for S1, position1, is in the "off" position.

S1 – Position 2

S1, position 2, is for data carrier detect (DCD). If position 2 is set in the "on" position, the CP8xxx board will reset the CPU when there is a loss of carrier. The factory default setting for S1, position 2, is in the "off" position.

Table 1 defines the switch positions for S1.

Table 1 S1 Switch Settings

Function of Reset Control Switch (S1)	1	2
Reset on Loss of DSR	On	
Do Not Reset on Loss of DSR	Off	
Reset on Loss of DCD		On
Do Not Reset on Loss of DCD		Off
Factory Settings	Off	Off

Jumper Settings

JP1 and JP5 – On-Board Ethernet Controller/Jumper Settings

The board is equipped with two integrated Intel® 82559 PCI fast Ethernet controllers with two RJ-45 10/100 BASE TX connectors on the mounting bracket at the rear of the board. The I/O addresses and interrupts are set by the PCI plug and play BIOS at boot time. The controllers are enabled or disabled via jumpers JP1 and JP5 (see Figure 2 for jumper locations).

JP1 corresponds to the Ethernet controller and the Ethernet port farthest from the processor. JP5 corresponds to the Ethernet controller and Ethernet port closest to the processor. For unique situations requiring the disabling of the Ethernet controllers, JP1 and JP5 are incorporated onto the CP8xxx board.

Table 2 defines the jumper settings for JP1 and JP5.

Table 2 Ethernet Jumper Settings for JP1 and JP5

Jumper	Function	Jumper On Pins 1-2	Jumper On Pins 2-3
JP1	Ethernet	Enabled	Disabled
JP5	Ethernet	Enabled	Disabled

JP2 – CMOS Memory Clear

The CMOS memory can be cleared by using JP2 (see Figure 2 for JP2 location). This memory controls the maintenance and storage of three sets of information: (1) the date and time generated and displayed on the computer screen; (2) the peripheral setup, i.e. programming base register for the chip sets; and (3) the password necessary for entry.

The first two sets of information can be changed during boot-up by following specific directions displayed on the computer screen at the time the computer is booting-up. The CMOS memory will automatically update and store the new information input. However, if setup cannot be entered the normal way, CMOS memory clear (JP2) is the recovery mechanism which can be used. Or, if password information has been lost, the CMOS memory will need to be cleared so the information can be updated, before program entry is possible.

To clear CMOS memory, the jumper on JP2 must be removed from pins 1 and 2, and placed on pins 2 and 3. After clearing, the jumper must be reinstalled on jumper pins 1 and 2 before updates can be made.

Table 3 defines the jumper settings for JP2.

Table 3 CMOS Clear Jumper Settings for JP2

Jumper	Function	Jumper On Pins 1-2	Jumper On Pins 2-3
JP2	CMOS Clear	Normal	CMOS Clear

JP3 – Flash Bios Enable

If the Flash Bios is to be upgraded, a shunt must be installed on the 2-pin jumper JP3 (see figure 2 for JP3 location). Upgrades typically come on a floppy disc and are accompanied by upgrade instructions .* When the upgrade is complete, the shunt should be removed to protect the system from accidental erasure.

Table 4 defines the jumper settings for JP3.

Table 4 Write Enable/Flash BIOS Jumper Settings for JP3

Jumper	Function	Jumper On	Jumper Off
JP3	Flash Write Enable	Enabled	Disabled

*Cubix provides Flash Bios upgrades via the Cubix web site. The web site address is provided in Appendix A of this manual.

JP4 – IES Interrupt on IRQ10

The IES module communicates with the CP8xxx processor in the subsystem via a hardware interrupt which is IRQ10. The supervisory interrupt is enabled with JP4 by placing the jumper on pins 2 and 3. If the CP8xxx board is part of the GlobalVision network, supervisory interrupt is necessary and IES Interrupt must be enabled. If this board is not part of the GlobalVision network, IES Interrupt can be disabled with JP4 by removing the jumper from pins 2 and 3, and placing the jumper on pins 1 and 2. The factory default setting for JP4 is in "disabled" status, unless otherwise specified at the time of purchase.

Table 5 defines the jumper settings for JP4.

Table 5 Enable/Disable IES Interrupt Jumper Settings for JP4

Jumper	Function	Jumper On Pins 1-2	Jumper On Pins 2-3
JP4	IES Interrupt on IRQ10	Disabled	Enabled

Symbios SCSI Controller/Jumper Settings

The CP8xxx board comes equipped to support an internal IDE drive. However, for applications that require external SCSI devices, an integrated Wide Ultra2 SCSI controller (Symbios 53C895) and an external SCSI cable connector (68-pin) can be ordered as an option. This SCSI controller supports both LVD and Single-Ended SCSI devices. The controller is enabled or disabled via a hardware jumper SJP1. (The "S" preceding the "JP" designates the jumper is specific to SCSI functions.)

The SCSI controller is a bus master device which gains control of the PCI bus to transfer data between the CPU memory and the SCSI devices. The I/O base address and interrupts are set by the PCI plug and play BIOS at boot time.

If the SCSI controller is ordered, a SCSI configuration utility is available on boot-up of the board. Shortly after the SCSI BIOS information displays, the configuration program can be accessed by pressing "Control C". The configuration utility will allow you to scan the SCSI bus, change configuration options and view a list of SCSI devices connected to the board.

SJP1 – Enable/Disable SCSI Controller

As stated above, the on-board Symbios Wide Ultra2 SCSI controller can be enabled or disabled with SJP1 (see Figure 2 for SJP1 location).

Table 6 defines the jumper settings for SJP1.

Table 6 SCSI Jumper Settings for SJP1

Jumper	Function	Jumper On Pins 1-2	Jumper On Pins 2-3
SJP1	SCSI	Enabled	Disabled

The SCSI controller supports up to 15 external SCSI hard drives, either Ultra2 LVD SCSI or Single-Ended Wide SCSI devices. The end of the SCSI chain must be terminated independent of whether drives are single-ended or LVD. Consult the owner's manual pertaining to the external SCSI device for instructions on how to terminate. The end of the SCSI chain **must be terminated** independent of whether drives are Single-Ended or LVD.

Figure 3 demonstrates SCSI termination enabled on the CP8xxx board, and termination of the external SCSI device at the end of the SCSI chain.

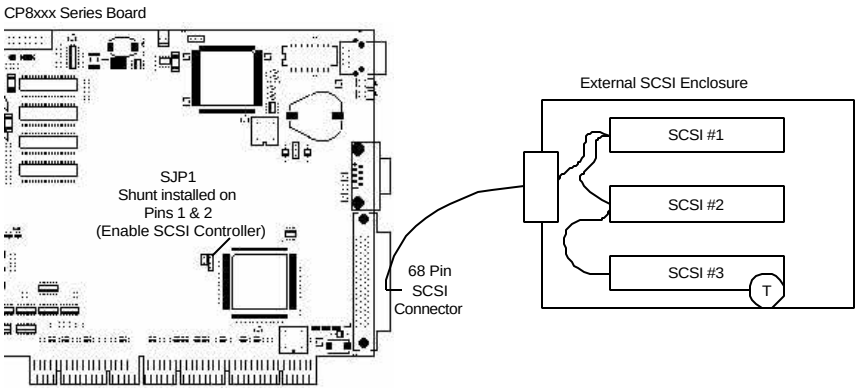

Figure 3 Configuration for Use of External SCSI Devices

DIMM MEMORY INSTALLATION

Additional memory can be installed on the CP8xxx board. There are two DIMM slots available on this board (see Figure 2 for DIMM slot locations). If only one DIMM is installed, this DIMM should be installed in DIMM 0 (J5). The sequence of DIMM installation relative to DIMM size is not important. DIMMs must be PC-100 compliant.

For installation, the card interface tabs must be aligned. Firmly seat the DIMM(s) into place.

Please note the following information regarding DIMMs.

- DIMMs are 168 pin, 100MHz (PC100) ECC SDRAM (72 bits).
- DIMMs do not need to be installed in pairs and different sizes may be mixed.
- DIMMs may be either registered or unbuffered. Registered and unbuffered DIMMs may not be mixed.
- DIMMs must have gold contacts (edge connectors).

Chapter 3 – Warnings and Board Installation Procedures

WARNINGS

The installation of processor boards requires entry into the CPU bay of the Density Series system which is restricted to qualified service personnel only. Accordingly, the following warnings apply.

CAUTION!
CONTAINS HAZARDOUS VOLTAGES
NO USER SERVICEABLE PARTS

ATTENTION!
TENSION DANGEREUSE, L'APPAREIL NE COMPORTE AUUN ELEMENT QUE L'UTILISATEUR PULSSE REPARER

ACHTUNG!
GEFAHRLICHE STROMSPANNUNGEN!
KEIN BENUTZER QUGANGLICHE TEILE!

CAUTION!
Group power must be off before installing any Cubix processors, peripheral boards, or third-party peripheral cards. Failure to follow this warning may result in damage to the Density Series system and boards being installed.

BOARD INSTALLATION

The following steps guide through the installation process.

1. At the front console, select and turn power off to the group location where you intend to install the server board.
2. If a hard-drive is installed in the group hard drive slot, remove the hard drive.
3. Confirm the switch and jumper settings are correct on the board being installed.
4. Insert the board into the group slot, ensuring the card interface tabs are aligned with the center of the slot (see Figure 4).
5. Firmly seat the processor card into the slots by firmly pressing on the top of the card with the palm of your hand.
6. Install the hard drive assembly into the appropriate hard drive bay located in the front of the Density enclosure. The hard drive assembly will fit into the hard drive interface. Press firmly to seat.
7. Connect all appropriate ribbon connectors and L-bracket connectors.
8. At the front of the console, apply power to the processor group.

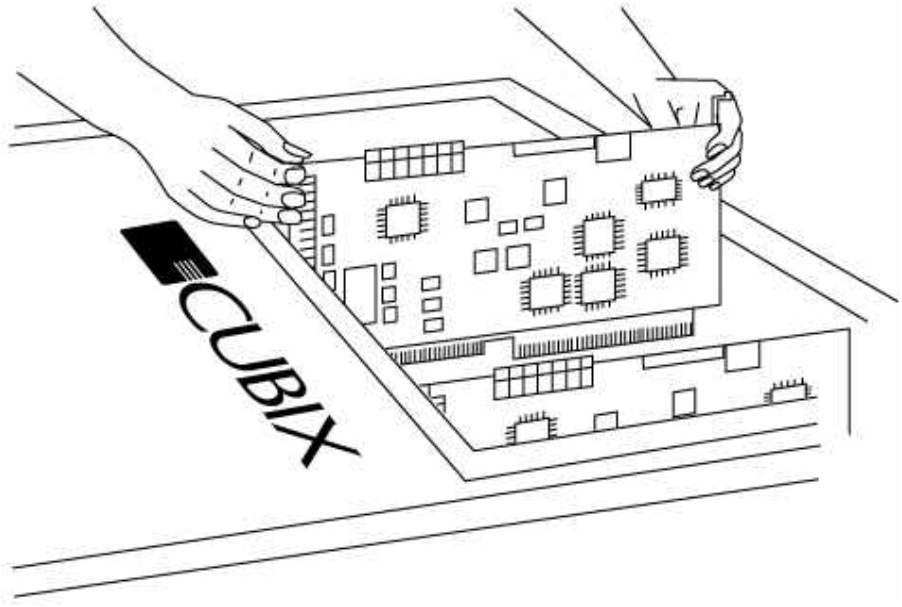

Figure 4 Inserting Server Board into Chasis Group

Chapter 4 – CP8xxx Board Information and Technical Specifications

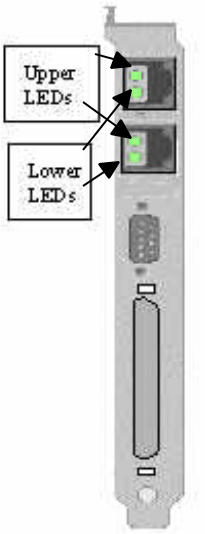

Figure 5
CP8xxx
End Bracket

ETHERNET ADAPTER LEDs

On each RJ-45 connector and visible in the mounting bracket is a set of light emitting diodes (LEDs). Figure 5 displays the CP8xxx end bracket.

On the upper LED:

- When the upper LED is green and blinking, this indicates a link to an Ethernet hub and that when blinking, there is activity.

On the lower LED:

- When the lower LED is green, this indicates the interface is set to 100 Mbit/s.

OTHER LEDs

POST Display

The CP8xxx board has a group of eight LEDs arranged above the IDE connector (J9). As the system proceeds through its Power On System Test (POST) these LEDs display binary codes which can be used to diagnose board failures. Refer to the AMIBIOS POST Checkpoint Codes (Doc. #0882) for detailed POST code information, or check the Cubix website:

http://www.cubix .com

CP8xxx Board Power LED

There is a Board Power LED light located on the CP8xxx board between COM2 (J3) and the LPT connector (J4) (see Figure 2 for Board Power LED location). This LED light will be green when there is power to the board. This LED is only visible when the cover is off of the Density System.

SCSI Activity LED

There is a SCSI Activity LED light on the back side of the CP8xxx board. This light will be amber when the SCSI is busy. The SCSI Activity LED is located at the rear of the board, close to the Ethernet Enable Jumper (JP1) legend, and is only visible when the cover is off of the Density System.

MEMORY CONFIGURATION & MANAGEMENT

Table 7 shows the Memory map for the CP processor.

Table 7 Memory Map

Memory Range	Size	Use
00000-9FFFF	640KB	Conventional Memory
A0000-AFFFF	64KB	VGA Graphics Buffer
B0000-B7FFF	32KB	MDA Text Buffer
B8000-BFFFF	32KB	VGA/CGA Text Buffer
C0000-C7FFF	32KB	VGA Bios
C8000-DFFFF	96KB	Available
E0000-FFFFF	128KB	System & PCI BIOS

Table 8 defines the board's I/O configuration.

Table 8 I/O Map

ISA Ports	Description
0000-00FF	Various "AT" functions in ISP chip and keyboard controller
01F0-01F7	IDE hard drive interface
02F8-02FF	COM2
03A0	Cubix supervisory interface
03A8-03AF	IES serial port
03B4-03B5	VGA
03BC-03BF	LPT1
03C0-03CF	VGA
03D4-03D5	VGA
03F0-03F7	Floppy / IDE
03F8-03FF	COM1

System Interrupts

The 16 system hardware interrupts on the CP8xxx are represented in Table 9. Interrupts are managed by two standard 8259A Programmable Interrupt Controllers (PICs) integrated into the chipset. Interrupts at IRQ 0 through 7 are located on the main PIC; IRQ 8 through 15 are on the SLAVE PIC.

Table 9 defines the system interrupts on the CP8xxx board.

Table 9 System Interrupts

IRQ	Description	IRQ	Description
0	Timer clock	**8**	Real Time Clock
1	Keyboard	**9**	Redirected IRQ 2, Set By PCI Plug & Play at Boot Time
2	Second PIC controller	**10**	Reserved for IES (Factory Default, see JP4)
3	COM2	**11**	Set By PCI Plug & Play at Boot Time
4	COM1	**12**	Available (or PS/2 Mouse)
5	Set By PCI Plug & Play at boot time	**13**	Math Coprocessor
6	Floppy Disk Controller	**14**	Primary IDE
7	LPT1	**15**	Secondary IDE Controller (CD-ROM)

TECHNICAL SPECIFICATIONS

Table 10 represents the technical specifications for the Density CP8xxx Series board.

Table 10 Technical Specifications for Density CP8xxx

CPU – Central Processing Unit	Intel® Celeron 500MHz		
L2 Cache	128KB Full Speed (Processor Dependent)		
System Chip Set	440BX PIIX 4E		
System Memory			
Speed	PC-100 SDRAM		
Width	72 Bits ECC		
Max Size	512MB, 2 – 256KB DIMMS		
Type	Unbuffered or Registered, DO NOT MIX		
Peripheral Bus Support	PCI or ISA		
System BIOS	AMI BIOS		
Super I/O	SMC 37C669		
Serial/Assignment	COM1 (J11), COM2 (J3)		
UART Type	16C550 Compatible 230 Kbps Maximum		
Parallel/Assignment	LPT 1 (J4), all Standard Modes		
Dual On-Board LAN Interface	RJ-45 10/100 Base TX, Intel®82559		
VGA Chip Set	S3 Trio 3D/2X, 4MB Video RAM		
SCSI Chip Set	Wide Ultra2 SCSI Symbios 53C895 with Low Voltage Differential or Single-Ended SCSI support (external connector only)		
Max Transfer Rate	Single-Ended 40MB, LVD 80MB		
Other Input/Output	Video/Keyboard/Mouse – (J2) Internal Header		
Power Requirements* *Does not include power for IDE Hard Drive	Volts +5VDC +12VDC -12VDC	Amps Max 7.6A 0.25A 0.05A	Power Max 41.6W
Warranty	Parts and Labor Return to Manufacturer 3 yrs.		

APPENDIX A

CUSTOMER SERVICE INFORMATION

For Customer Service Information: 1-800-829-0551

Customer Service available from:

5:00 a.m. to 5:00 p.m. PST Monday through Friday
Also, from 8:00 a.m. to 4 p.m. PST on Saturday
Closed holidays and holiday weekends

Use the Cubix Web site for trouble-shooting aids and for access to the latest information on Cubix products.

Customer Service Web site: http://www.cubix.com/support

Customer Service Email address: customerservice@cubix.com